**Muhammad Aldacher**  
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**OBJECTIVE**

Analog & Mixed-Signal design engineer looking for a challenging opportunity in circuit design, where I can apply my three years of industry experience designing circuits like PLLs, ADCs, RF Receivers, and OpAmps to develop the next generation of circuits in advanced submicron technologies.

**EDUCATION**

**San Jose State University,** San Jose, CA

M.S., Electrical Engineering, **Current GPA 4/4** Aug 2016 – Present

*Coursework*: Analog Integrated Circuits, RF Integrated Circuit Design I, Digital Design with FPGAs,High speed CMOS design,  
 Data Conversions in AMS ICs, RF Integrated Circuit Design II

**Alexandria University, Faculty of Engineering**, Alexandria, Egypt

Graduate coursework, Electrical Engineering, **GPA 4/4** Sep 2014 – Dec 2015  
 *Coursework*: Nanotechnology Basics, Solid-State Physics, DSP Architecture & Circuits, Wave Propagation in Biological media.

B.S., Electrical Engineering, Electronics Major, **GPA 3.96/4** Sep 2008 – Jun 2013  
 Distinction with degree of honor & Rank in the top ten.

**WORK EXPERIENCE**

**Xilinx Inc.**, San Jose, CA

*Analog & Mixed-Signal IC Design Engineer* Jan 2019 – Present

* Designing **PLL** circuits in 7nm for Xilinx’s Versal chip & other programmable products.
* Responsible for post-layout reliability analysis including EM/IR simulations and Guardring checks using Ansys Totem.
* Developing post-silicon test automation environments to test PLL circuits’ functionality, jitter, & noise performances across PVT.
* Created VerilogA models to simulate the behavior of the fractional modes and the spread-spectrum feature of the PLLs.
* Created Verilog patterns to test different PLLs on the FPGA through Vivado design suite software.

**STMicroelectronics**, Santa Clara, CA

*Device Validation Engineer (Analog & Mixed-Signal)* Feb 2017 – Jan 2019

* Responsible for post-silicon validation of **PreAmp** & **Motor driver** ASICs, including functional, performance, & corner analyses.
* Developed fully-automated testbenchs to validate the performance of different parts of the PreAmp.
* Responsible for test plan development & for test automation through VB.NET scripts.

**RFIC Lab, San Jose State University,** San Jose, CA

*Research Assistant* Feb 2017 – Jan 2018

* Worked on the tape-out of a Bluetooth Low Energy (BLE) based front end Receiver in 65nm CMOS technology.
* Designed high-speed circuits using the nanowire SGFET technology.

**CURRICULUM PROJECTS**

*“1.9 GHz PLL with LC VCO”* Oct 2018 – Dec 2018

* Designed a 2nd order PLL with a bootstrapped charge pump & an LC VCO achieving rms jitter of 1.54 ps & an FOM of -235 dB.

Using VerilogA & Matlab, the PLL is modelled to achieve a phase margin of 56O, a BW of 1.4 MHz, & a locking time of 2 us.

*“50 MS/s 10-Bit Pipeline ADC”* Mar 2018 – May 2018

* Designed a 1.5-bit ADC consisting of a 2-stage comparator & a switching-capacitor MDAC with a gain-boosted telescopic OpAmp. Taking a 64-point FFT on the output in 2x-gain mode, ENOB achieved = 9.756 bits, SNR = 60.495 dB & total power = 2.0286 mW.

*“ADC & DAC Behavioral Modelling”* Jan 2018 – Feb 2018

* Modelled a 10-bit Pipeline ADC with digital correction & a 4-bit Flash ADC with DACs, using ideal components & using VerilogA.

*“Digital & Analog Clock Display using Digilent Basys3 Artix-7 FPGA”* Oct 2017 – Dec 2017

* Designed a clock whose seconds, minutes, & hours are displayed on a Quad 7-segment display. Picoblaze processor is used to control the Analog & Digital displays of the clock on a VGA display.

*“8x8 6T-SRAM Array with 3-8 row decoder”* Oct 2017 – Dec 2017

* Designed the layout of an 8x8 SRAM Array in TSMC 65nm CMOS with Read SNM = 0.24V, Write SNM = 0.36V, & Area = 1883um2.

*“1 GHz Low-Power Dynamic Comparator” (Published in ICECS’17)* Jan 2017 – Jun 2017

* Designed a 2-stage double-tail Dynamic Comparator in TSMC 65nm CMOS with Resolution = 327nV, Delay = 272ps, & P = 220uW.

*“10 GHz PLL using SGFET technology”* *(Published in NGCAS’17)* Oct 2016 – Dec 2016

* Implemented a 10.3GHz Charge Pump PLL using nanowire SGFET technology, with a tuning range = 3GHz–14GHz, & P = 35uW.

*“High FoM 2.4 GHz Bluetooth LNA”* Oct 2016 – Dec 2016

* Designed a CS LNA in the 45nm CMOS process with Gain of 15dB, NF of 5.86dB, P1dB of -13.4 dBm, & |S11| of -12.8dB.

*“PLL for a High-Speed Serial link Transceiver”* Sep 2012 – Jun 2013

* Designed a PLL system for 10GbaseKR transceiver in 65nm CMOS process, with rms jitter of 47 fs & bandwidth 7 MHz.

*“8-bit CMOS Microprocessor design”* Mar 2013 – Jun 2013

* Implemented the behavioral model of an 8-bit microprocessor using Verilog & its layout using L-Edit.

*“CMOS OpAmp design”* Jul 2012 – Sep 2012

* Designed 2-stage amplifier in 180nm CMOS process, with voltage gain of 46 dB, bandwidth 21.9 MHz, & CMRR 25.8 dB.

**TECHNICAL SKILLS**

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| * **Simulation Tools:** Cadence Virtuoso, HSpice, WaveView, XA | * **Programming:** VB.NET, Python, C, Matlab |
| * **HDLs (RTL):** Verilog, VHDL, VerilogA | * **FPGA Design Tools:** Xilinx Vivado |
| * **Layout:** Cadence Virtuoso, L-Edit, Electric | * **Physical Verification:** LVS, DRC, Density rules |
| * **Microcontrollers:** Arduino, AVR | * **Lab Equipment:** Network Analyzer, TDR, AWG, DSA, Oscilloscope, Multimeter, Function generator, Spectroscope |

**PUBLICATIONS**

*"A Low-power, High-resolution, 1 GHz Differential Comparator with Low-Offset and Low-Kickback"*

[**Aldacher**](http://link.springer.com/search?facet-creator=%22M.+Aldacher%22)**,M.**, Nasrollahpour, M., Hamedi-Hagh, S.

IEEE International Conference on Electronics, Circuits and Systems (ICECS), 2017, DOI: 10.1109/ICECS.2017.8292027

*“Design & Analysis of a nanowire SGFET-based 10GHz Frequency Synthesizer”*

**[Aldacher](http://link.springer.com/search?facet-creator=%22M.+Aldacher%22),M.**, Hamedi-Hagh, S.

New Generation of Circuits and Systems Conference (NGCAS), 2017, DOI: 10.1109/NGCAS.2017.50

*“Bluetooth Low Energy(BLE) based Direct down conversion Receiver Front End in 65nm CMOS”*

Nasrollahpour, M., Sreekumar, R., Hajilou, F., [**Aldacher**](http://link.springer.com/search?facet-creator=%22M.+Aldacher%22)**,M.**, Hamedi-Hagh, S.

New Generation of Circuits and Systems Conference (NGCAS), 2017, DOI: 10.1109/NGCAS.2017.44

*“Parametric study of up-conversion efficiency in Er-doped lanthanide hosts under 780/980 nm excitation wavelengths”*

[Samir](http://link.springer.com/search?facet-creator=%22E.+Samir%22),E., [Shehata](http://link.springer.com/search?facet-creator=%22N.+Shehata%22),N., [**Aldacher**](http://link.springer.com/search?facet-creator=%22M.+Aldacher%22)**,M.**, [Kandas](http://link.springer.com/search?facet-creator=%22I.+Kandas%22),I.

Journal of Electronic Materials, 2016, DOI: 10.1007/s11664-015-4331-2

*“Parametric study of up-conversion efficiency in Er-doped ceria nanoparticles under 780nm excitation****”***

[Shehata](http://link.springer.com/search?facet-creator=%22N.+Shehata%22),N., [Kandas](http://link.springer.com/search?facet-creator=%22I.+Kandas%22),I., [Samir](http://link.springer.com/search?facet-creator=%22E.+Samir%22),E., Meehan,K., [**Aldacher**](http://link.springer.com/search?facet-creator=%22M.+Aldacher%22)**,M.**

Journal of Luminescence, 2016, [DOI: 10.1016/j.jlumin.2016.03.013](http://dx.doi.org/10.1016/j.jlumin.2016.03.013)

**ACTIVITIES**

First Focus Learning Center, Mountain View, CA

* Arduino *& Basic Electronics Instructor* (2016)

Alexandria University, Alexandria, Egypt

* *Head of the Marketing committee* **–** IEEE Alexandria University Student Branch (2011 – 2014)
* *Vice-Chairman & Head of the Marketing Committee* **–** Egypt Scholars Inc. | Alex. Univ. SC (2013 – 2014)
* *Cofounder & Board member* **–** E-WEB Scientific Association (2011 – 2012)